Microstructures

Perspective

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Roadmap for ferroelectric domain wall memory

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How to cite this article: Sun J, Li Y, Hu D, Shen B, Zhang B, Wang Z, Tang H, Jiang A. Roadmap for ferroelectric domain wall memory. *Microstructures* 2024;4:2024007. https://dx.doi.org/10.20517/microstructures.2023.52

Received: 25 Sep 2023 **First Decision:** 24 Oct 2023 **Revised:** 23 Nov 2023 **Accepted:** 7 Dec 2023 **Published:** 12 Jan 2024

Academic Editor: Nazanin Bassiri-Gharb **Copy Editor:** Fangyuan Liu **Production Editor:** Fangyuan Liu

Abstract

Commercial nonvolatile Ferroelectric Random Access Memory employs a destructive readout scheme based on charge sensing, which limits its cell scalability in sizes above 100 nm. Ferroelectric domain walls are two-dimensional topological interfaces with thicknesses approaching the unit cell level between two antiparallel domains and exhibit electrical conductivity, distinguishing them from insulating matrices that are uniformly ordered. Recently, novel research has been devoted to utilizing this extraordinary interface for the application in nonvolatile memory with nanometer-sized scalability and low energy consumption. Here, we pay more attention to the development of the domain wall memory technologies in the future with challenges and opportunities to design planar and vertical arrays of the memory cells in the CMOS platform.

Keywords: Ferroelectric, domain wall, memory, 1T1R, crossbar

INTRODUCTION

With the advent of the era of big data and the Internet of Things (IoT), the traditional von Neumann computing architecture leads to exponential growth in data throughput between processing units and main memory and between main memory and storage, resulting in significant power consumption and signaling delays[1]. Furthermore, this limitation is expected to exacerbate due to the physical separation between memory and logic units and the increasing speed gap between the central processing unit (CPU) and the CPU off-chip memory[2,3]. To overcome the limitations of the von Neumann architecture, a variety of nonvolatile memories (NVM) are emerging, including resistive random access memory (RRAM),

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Sun *et al. Microstructures* 2024;4:2024007 | https://dx.doi.org/10.20517/microstructures.2023.52

magnetoresistive RAM (MRAM), phase change RAM (PCRAM), and ferroelectric RAM (FeRAM)[4]. These emerging NVMs aim to create memory/storage devices with characteristics such as high speed, high reliability, low power, high capacity, and compatibility with complementary metal-semiconductor fabrication technologies. However, so far, none of these emerging technologies meet all requirements simultaneously, and their market occupations are rare in comparison to the DRAM and vNAND.

FeRAM has excellent characteristics, such as nonvolatility, high write speed, low power consumption, high fatigue resistance, and high irradiation protection, making it a promising candidate for various applications[5-7]. Since 2000, FeRAM commercial products have been found in the memory card of Sony's PlayStation 2, smart debit cards, and telecommunications[8]. However, one of the major drawbacks is its low storage capacity (4-8 MB), which significantly constrains the development of high-capacity and high-density memory markets. The traditional FeRAM technology node remains stuck at 90-130 nm due to the bottleneck of a charge sensing-based destructive readout scheme[9,10].

Since the discovery of ferroelectricity by Valacek in 1921[11], ferroelectric domains have been considered as fundamental entities of the ordered dipoles in electronic devices, driving their development in information storage. However, it was not until 2009 that ferroelectric domain walls in thin films were verified to possess enhanced electrical conductivity[12], which led to their emergence as a new current readout technique of nanometer-sized domains to receive rapid development in the last decade [Figure 1]. Ferroelectric domain walls possess the polarity order and agile topological interfaces and allow an electric field to selectively control their positions, conformations, and functions in time, resulting in conduction distinct from their surrounding bulk[13]. Distinguished from the destructive charge readout scheme of conventional FeRAMs, the current readout technique arising from conducting domain walls has been developed in several research groups that are expected to miniaturize ferroelectric memory devices to achieve the high-capacity storage significantly.

As the Nobel Prize-winning physicist Herbert Kroemer famously said[14], "The interface is the device". Ferroelectric domain walls could revolutionize nanoscale electronics beyond traditional device architectures, making ferroelectric domain wall memories an excellent candidate among NVMs. To advance the development of this field further, we reexamine the prospects of ferroelectric domain walls in high-density information storage, including challenges and opportunities, and discuss several commercialization paths in the future.

DOMAIN ENGINEERING

Ferroelectric materials have spontaneous polarizations P_s that can be reversibly switched between two or more directions (polarities) by applying an external field owing to energy degeneracies of multiple equilibrium states. Two adjacent domains in different orientations are separated by domain walls[15]. The angle between them can affect the domain wall current. Therefore, there are many studies focused on domain engineering[16-19] (e.g., domain orientation and domain dimensions) or domain wall engineering[20-23] (e.g., domain wall mobility, topology, and domain wall conduction). Specific strategies of ferroelectric domain/domain wall engineering include chemical modification, electrostatic boundary control, strain engineering, substrate engineering, *etc.*, which can be specifically classified according to their intended purpose and the materials involved. This section summarizes domain engineering technologies and related domain wall functions for several typical ferroelectric materials, with a special focus on the modulation of ferroelectric-related properties.

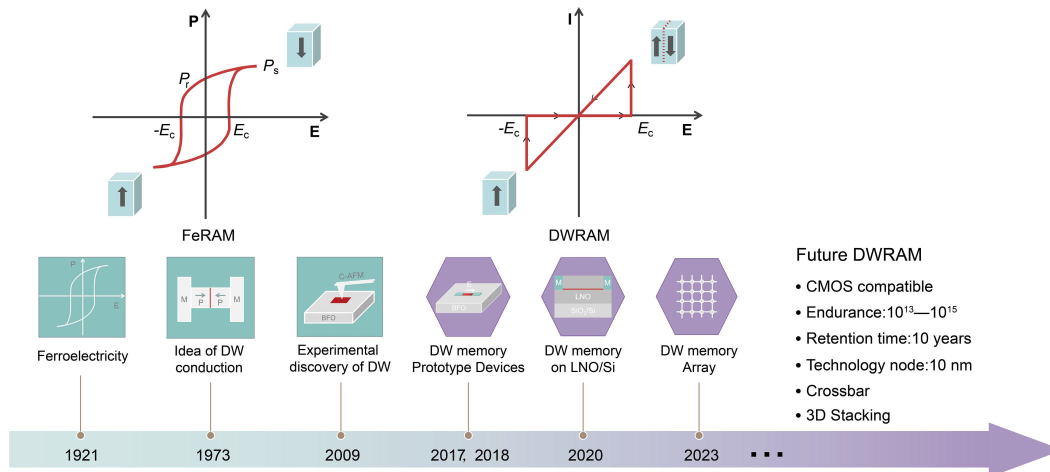

Figure 1. Chronological development of ferroelectric domain wall memory (DWRAM).

Proto-type bismuth ferrite ($BiFeO_3$, BFO) ferroelectric thin films have been the most thoroughly studied since their high wall conduction was discovered in the last century. Depending on the angular difference between neighboring domains, there are three types of domain walls in the BFO: 71°, 109°, and 180°. In general, the 180° domain wall is purely ferroelectric, while the 71° and 109° domain walls are both ferroelectric and ferroelastic[24]. Domain engineering can be achieved by various methods, such as strain, doping, electric field, magnetic field, temperature, light, or interface engineering. These methods can alter the domain structure, phase transition, domain wall motion, or domain wall properties, resulting in enhanced wall currents or the appearance of novel functionalities. The use of epitaxial substrate matching strain has been proved to be an effective way to modify BFO domain symmetry, enhance polarization, and induce a transition from a tetragonal (T) into a rhombohedral (R) phase where the spontaneous polarizations along the <111> directions show limited sensitivity to the substrate strain but have strain-induced rotation rather than amplitude change[25]. A reversible transition from R-like to T-like domain symmetry occurs under an increasing compressive strain, which is attributed to the large displacement of Bi, Fe ions and the oxygen octahedrons along the [001] directions, leading to a giant polarization[26]. As the BFO film thickness exceeds 30 nm, the T-like domains can transform into R-like/T-like mixed domains with periodic stripe-like structures, along with the relaxation of the substrate strain[27,28]. The resulting complex domain structures offer opportunities to modify BFO's walls and their conducting behaviors. Additionally, the domain variants can be efficiently tuned by a vicinal substrate. It is reported that the BFO films in step-flow growth modes on 4° miscut $SrTiO_3$ [110] substrates can easily form two-variant striped domains while maintaining high polarizations and low coercive fields[29]. The large number of domain boundaries can increase the wall current.

One key performance related to the domain wall devices is retention. In the case of the BFO domain wall memory devices, potential performing instabilities originate from the depolarization field and the ferroelastic energy at the artificially created domain wall regions. Eliminating the constraints imposed by the surrounding region can significantly improve the stability of the switched polarization[30]. On the contrary, doping-induced structural defects can act as domain wall pinning centers that restrain the domain switching process. However, the co-doped BFO films can improve retention time over one year[31]. In recent years, topologically structured domain states, such as vortex and center-structured domains, have been observed in BFO nano-islands, which provide new opportunities for exploring and tuning the domain wall properties[32]. The domain structure can be reversibly switched between center-convergent and center-

divergent configurations in favor of the storage of four domain wall states within a single nano-island in various conductivities[24].

The lithium niobate ($LiNbO_3$, LN) single crystal is a well-known ferroelectric and receives wide applications in the fields of photonics, electronics, and optoelectronics. Over the last decade or so, the "smart cut" technology has matured for producing large-area nanometer-to-micrometer-thick LN films on 4-8 silicon wafers (LNOI) in high quality. Nowadays, the tailored domain patterns are commercially available to improve their electrical and optical properties. For example, the fabrication of quasi-phase-matched structures using periodically polarized LNOI or PPLNOI films[33] is applied not only to optical waveguide devices but also to the domain wall transistors and domain wall memories in the configuration of the neuromorphic hardware[34,35]. In theory, the LN possessing a uniaxial structure should readily produce neutral 180° domain walls. In practice, the domain walls in LN can be tilted to form charged walls (CDW), which depend on the dopant concentration, e.g., magnesium (tilting up to 0.3°)[36]. Inclined domain walls in head-to-head configurations can accumulate free electronic carriers, leading to an intrinsic rise in conductivity[37], and the conductivity of a head-to-head CDW (H-H CDW) is three to four orders of magnitude higher than that of a tail-to-tail CDW (T-T CDW)[38]. However, difficulties arise from the instability of CDWs, which typically have high depolarization energies. Therefore, it is necessary to find a strategy that compromises depolarization energy and conductivity. The inclined wall angle can also be tuned through bending or control of its subsurface topology to achieve multilevel information-storing states[13]. For example, by the control of subsurface geometries of the domains, the inclined wall angle in LN can be changed by the increase in the applied electric field so that the domain wall conduction is tunable in multilevel states[39].

In conclusion, the multifold domain engineering techniques of ferroelectric materials offer a wealth of possibilities to enhance domain wall conduction. The ongoing exploration of these methods not only contributes to a deep understanding of the physics of developing the domain wall microelectronics but also unlocks new avenues for the innovation of electronic devices, sensors, and other emerging optoelectronic devices.

TWO-DIMENSIONAL DWRAM ARCHITECTURES

After the idea of ferroelectric domain wall conduction was first proposed in bulk crystals in 1973[40], it took nearly four decades to find localized wall conduction within ferroelectric thin films, where Seidel *et al.* found conducting 109° and 180° domain walls within the rhombohedral phase of BFO thin films after current mapping of written domains using the conducting atomic force microscope (C-AFM) tip[12]. Solid-state memory devices were, thus, demonstrated under reversible injection and erasure of these conducting domain walls. Nowadays, the operations of ferroelectric domain wall memories can be categorized into in-plane and out-of-plane types depending on the written domain patterns within the films.

Out-of-plane DWRAM

The paradigmatic example of out-of-plane domain wall memories is using conductive domain walls in the center-type topological quadrant domains to appear in high-quality epitaxial BFO films, where different write voltages can generate different domain wall conduction states[41-43]. Piezoresponse force microscopy (PFM) and C-AFM images of the written domains showed the quad-domains within each self-assembled BFO nano-island in center-convergent, center-divergent, and vortex states. Figure 2A shows the schematic of the experimental setup during C-AFM and PFM mapping of the BFO nano-island arrays, where the 3D morphology of the nano-island arrays is superimposed on their C-AFM images. A typical nano-island vortex domain structure is shown in Figure 2B (upper panel), containing four quadrants of head and tail

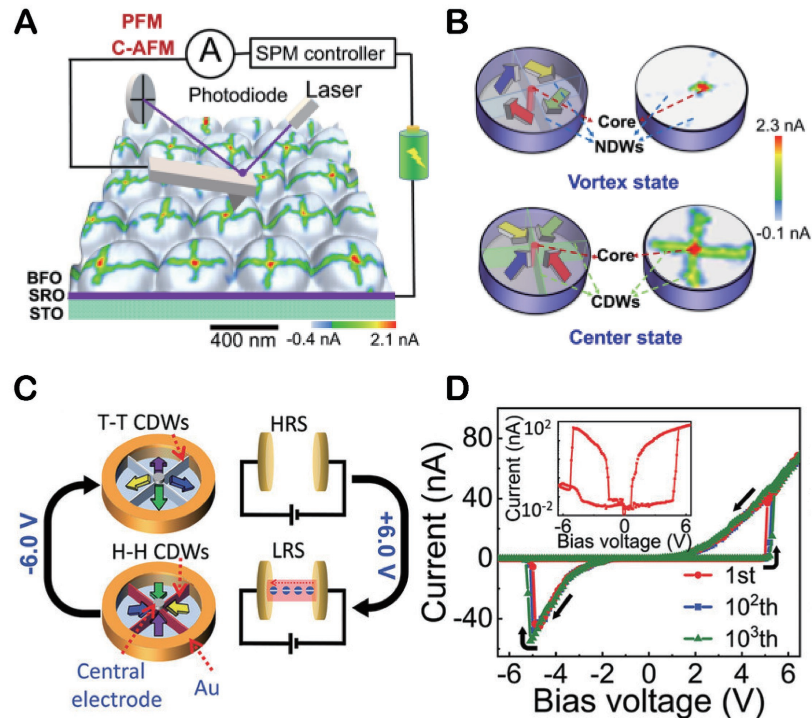

Figure 2. (A) The schematic of experimental setups during C-AFM and PFM mapping of an array of BFO nanoislands, wherein the 3D morphology of the arrayed nanoislands was superimposed with a C-AFM map of wall conduction. (B) The Schematic of domain structures in vortex and center states in different conduction patterns (C-AFM maps). Reprinted with permission[42]. Copyright 2021, Springer Nature. (C) The schematic of their working principle on the basis of creation and erasure of conducting domain wall states. Additionally, (D) demonstrates 1,000 sweeps of quasi-static *I*-*V* curves between -7 and 7 V. Inset shows an *I*-*V* curve in a semi-logarithmic plot. Reprinted with permission[43]. Copyright 2022, Wiley.

domains that form a transverse flux-closed vortex structure. Figure 2B (lower panel) shows a typical nano-island possessing centrally convergent domains with the transverse polarization components pointing toward the center in the formation of four H-H CDWs that meet in the core region[42]. With the use of these nano-islands, Yang *et al.* fabricated prototypical domain wall storage units embedded in a centered quadrant topological domain structure, where the divergent and convergent states can be switched back and forth[43]. The divergent state contains a T-T CDW in low conductivity in contrast to the convergent state of a H-H CDW in higher conductivity, as shown in Figure 2C. This type of storage device possesses a bipolar switching state [Figure 2D] in an on/off ratio of 10^4. Owing to the "protection" from the clamped topological ferroelastic quadrant domains, the written domains exhibited a long retention time of 10^6 s and high endurance cycles up to 10^8[43]. Further, the switchable domain wall states can be self-assembled within ferroelectric nano-islands and controlled by electric fields that can be applied to various logic gates (e.g., NOT, OR, AND, and their derivatives) and circuits (e.g., fan-out)[44]. The main challenge of out-of-plane domain wall memories arises from the high-temperature deposition of the epitaxial BFO films on the Si wafers, which are incompatible with current CMOS processes. Another consideration of this memory is the domain wall current (~40 nA), which is still insufficient to drive fast memory circuits.

In-plane DWRAM

For a ferroelectric thin film in a single domain pattern, in-plane prototype domain wall memory devices were realized on (110)-oriented BFO films using two-terminal coplanar electrodes. A C-AFM probe was employed to inject and erase a pair of isolated domain walls, setting the on and off states of the resistive

device in the presence or absence of the domain walls [Figure 3A][45]. The device allows noninvasive retrieval of coded data by reading the domain wall currents at low read voltages (0.5-2 V) in a ratio of > 10^3 [Figure 3B]. Once the written domains have poor retention, the cell can be etched into a mesa-like shape over the partial film thickness at the surface. After the deposition of two side electrodes to contact the cell, an in-plane write electric field is applied between the two side electrodes for the formation of two antiparallel and parallel domain patterns that have good retention. If the film has multidomains, an additional middle electrode was deposited at the surface between the two side electrodes to form a three-terminal cell, where the two side electrodes can be used to write a single domain pattern over the entire cell. The written information can be read out at a read electric field applied between the middle and one side electrodes. When the read field is opposite to the written polarization, domain walls come into forming via the local domain switching between the electrodes, resulting in a high read current (ON state). Otherwise, there is no domain switching and wall formation at the gap when the read field is parallel to the written polarization, and the read current is in an OFF state. The measured read current for the ON state was approximately 14 nA in ON/OFF ratios of approximately 100 and 3 for two- and three-terminal devices, respectively[46].

Unfortunately, the read current from the memory remains too low to satisfy the requirement of fast read/write circuits, besides the high fabrication temperature that arouses compatibility issues in the CMOS processes. Further experiments were conducted on planar mesa-structured memory cells using LN thin films that can be fabricated on the Si wafers at low temperatures via ionic implantation and chemical bonding technologies [Figure 3C]. The film has a single domain pattern, and each cell has a high ON/OFF ratio exceeding 10^6, with endurance cycles surpassing 10^{10}[47]. In a working principle identical to the above-mentioned two-terminal BFO memory, a writing field encodes the domain within the mesa parallel ("0") or antiparallel ("1") to the underlying reference domain in LN thin films. Between two antiparallel domains, a persistent 180° domain wall arises at the interface, enabling a high read domain wall current of 1 A flowing through a sub-20 nm memory cell[48]. Interestingly, a very thin layer that is generally known as the "dead" layer between the cell and side electrodes was found to function as an embedded selector for applications in memory computing[49], half-wave rectifiers[38,50], and crossbar structures[51]. Domain switching in these thin dead layers at the interface is volatile and results in transient domain walls during read operations when the read voltage is higher than the starting voltage (V_{on}) [Figure 3D and E].

To summarize, prototype devices for domain wall memories have been rapidly developed over the past few years and have demonstrated competitive nonvolatile storage performance [Table 1], driving the transition to chip-scale memories.

INTERCONNECTIONS: 1T1R AND CROSSBAR ARRAY

Although there have been many demonstrations of solid-state domain wall devices in recent years, large-scale integrated structures require further refinement before their commercialization. Most resistive memories (e.g., RRAM and PCM) employ crossbar architectures, where the memory materials are sandwiched between two planes arranged with mutually perpendicular word and bit lines. However, the disturbance of leaky circuit paths through neighboring cells can lead to the misreading of addressed cells. An effect solution is the integration of an additional selector (diode, selector, or transistor) in series with each memory cell to prevent such crosstalk effects[52-55]. Therefore, the 1T1R architecture is the most appropriate direction of early research for domain wall memories in bipolar conduction. Figure 4A and B sketches the 1T1R and crossbar architectures of out-of-plane and in-plane domain wall memories, respectively. In this setup, domain wall information is executed by the application of a write voltage to address word and bit lines. This scheme can be applied to self-assembled ferroelectric nano-islands to

Table 1. Benchmark performance comparison of various emerging memory devices

	FE-RAM	FE-FET	FTJ	PCRAM	RRAM	MRAM	DWRAM
Cell area	6-35 F^2	5-10 F^2	-	4-19 F^2	4-10 F^2	6-20 F^2	4 F^2
Non-volatility	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Write time	< 10 ns	< 100 ns	< 100 ns	< 100 ns	< 100 ns	< 20 ns	< 10 ns
Read time	< 10 ns	< 50 ns	< 50 ns	< 10 ns	< 10 ns	< 10 ns	< 10 ns
On/off ratio	-	10^5-10^6	> 10	> 10^3	> 10	> 2	10^5-10^6
Retention	> 10 years	> 10 years	> 10 years	> 10 years	> 10 years	> 10 years	> 10 years
Endurance	> 10^{14}	> 10^8	> 10^8	> 10^{10}	> 10^6	> 10^{12}	> 10^{10}

Data from refs.[1,38,47].

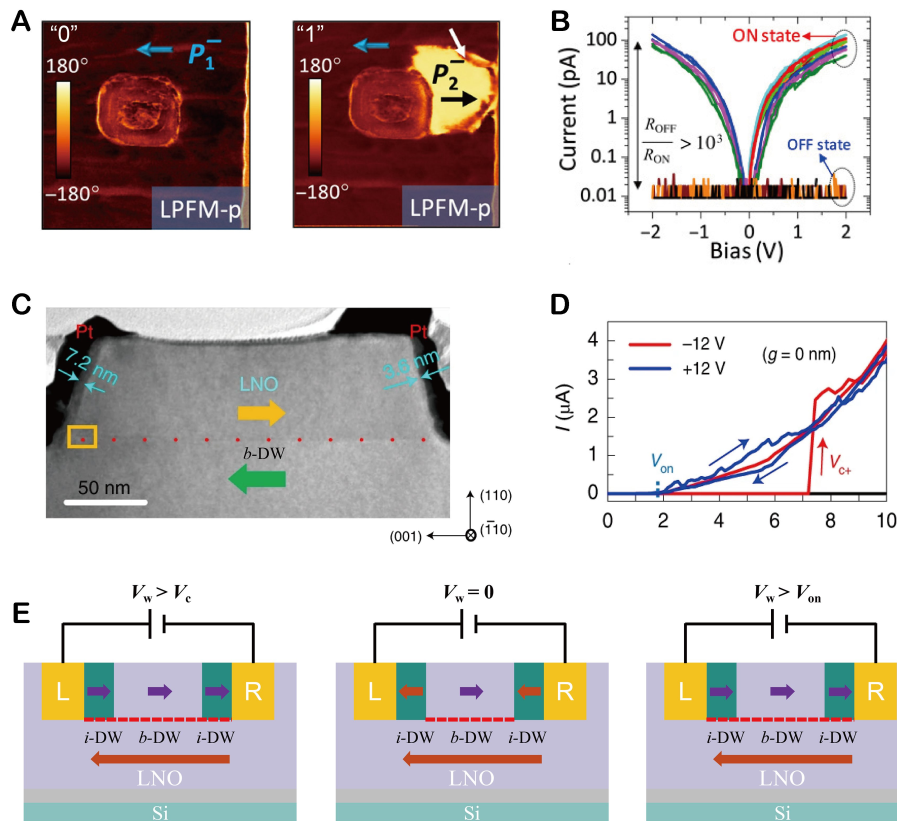

Figure 3. (A) Piezoresponse force microscopy (PFM) phase images of the erasable domain walls between two top electrodes. (B) *I-V* characteristics of the device in the presence ("1") and absence ("0") of domain walls. Reprinted with permission[45]. Copyright 2017, American Association for the Advancement of Science. (C) A cross-sectional TEM imaging of thin (3.6 and 7.2 nm) dead layers at the Pt-$LiNbO_3$ interfaces, where a red dotted line indicates a persistent domain wall between two antiparallel polarizations. (D) *I-V* curves after poling at +/-12 V for the generation of antiparallel and parallel domain patterns within a two-terminal LN cell, respectively. When $V > V_{c+}$ (7.2 V), the off current turns on abruptly implying the creation of a persistent domain wall via local domain 180° switching in formation of antiparallel polarization within the cell previously poled at -12 V. After the formation of antiparallel domain patterns after poling at +12 V, the off current turns on again at voltages above an onset voltage of 1.8 V ($V_{on} < V_{c+}$) due to the volatile domain switching within the thin interfacial layers. Reprinted with permission[47]. Copyright 2020, Springer Nature. (E) The working principle of the mesa-structured memory cell with two side electrodes fabricated on the surface of an X/Y-cut LN single-crystal film bonded to a silicon substrate. Nonvolatile bulk domain walls (b-DW) can encode the data in contrast to the volatile domain walls (i-DW) within the interfacial layers that work as an embedded selector.

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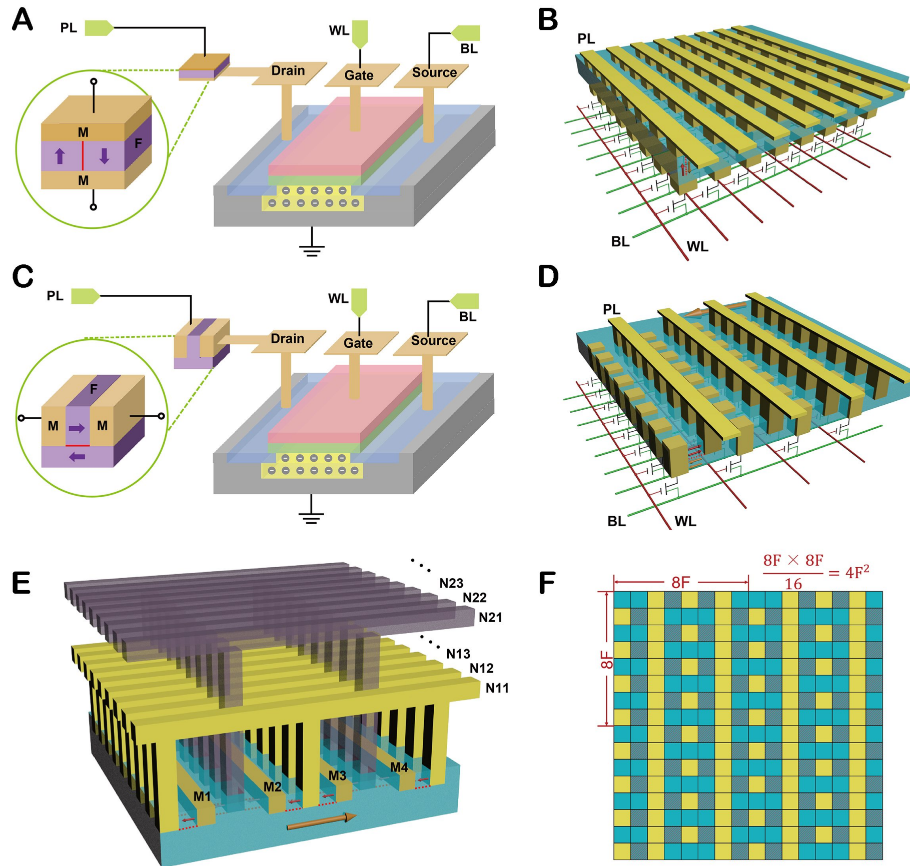

Figure 4. (A) The 1T1R structure of the out-of-plane DWRAM. (B) The crossbar architecture of the out-of-plane DWRAM. (C) The 1T1R structure of the in-plane DWRAM. (D) The crossbar architecture of the in-plane DWRAM. (E) Bird's-eye view of the LN DWRAM array. (F) Top-down view of the LN DWRAM array.

produce quadrants and/or centrally converging and diverging domain walls. However, the fast read requires a further increase of domain wall currents by at least two orders of magnitude. In consideration of large wall currents within LN single-crystal films, Similar 1T1R and crossbar architectures of in-plane domain wall memory are also proposed for LN in Figure 4C and D. Interestingly, the interfacial layers in preferred domain orientations offer an unparalleled advantage as embedded selectors to rectify unidirectional "on" currents just as those in diodes and anti-serial memristors, in operating speeds nearly identical to those of the intrinsic bulk domains. Figure 4E and F shows the interconnection of their dense arrays. The integration density can be further increased to $4F^2/i$ (i = 1, 2, 3, 4, ..., F-feature size) in the future by 3D stacking of these layers, where each cell can be addressed through the selection of one row and one column of the metal lines without affecting other cells.

3D ARCHITECTURE

In recent decades, the demand for high-capacity memory chips has surged significantly, driven by the rapidly expanding markets across various industries, including mobile devices, cloud services, and personal computers[56]. The rapid evolution of 3D NAND flash memory over the past decade has successfully catered to this increasing demand for market growth and enhanced performance. As of 2022, the eighth-generation 3D NAND flash memory has over 200 vertical gate stacks[56,57]. However, conventional NAND flash memory poses challenges due to its high operating voltage requirements (> 10 V) and limited endurance (< 10^4).

These limitations stem from repetitive tunneling of the oxide layer, which diminishes its insulating properties. Additionally, as device sizes shrink, parasitic capacitance effects in NAND flash become more pronounced, making it challenging to scale down below 20 nm[58]. Ferroelectric domain walls emerge as promising candidates to complete 3D NAND flash memory in the future. The advantages include the nanometer-sized scalability (domain wall thickness of ~1 nm), low voltage operation (< 2 V), and remarkable endurance cycles (> 10^{10})[13,59]. Furthermore, the reliable mechanism of ferroelectric domain walls plays a pivotal role in establishing a stable information storage channel, particularly in ferroelectric materials possessing a mature fabrication platform, such as lithium niobate crystals[60,61]. The reliable memory operation stems from the solid physics of the polarization reversal processing in three stages[60]: (i) critical domain nucleation; (ii) domain forward growth; and (iii) domain wall sideways motion, as illustrated in Figure 5A. The LN domain can grow up in a needle-like shape toward the opposite electrode under an in-plane applied electric field, as depicted in Figure 5B[62]. Therefore, the written domains can be highly conformed between the two side electrodes. This paves the way for the three-dimensional integration of ferroelectric domain wall memories. One strategy is the fabrication of periodic deep holes and trenches on the surface of a thick LN film. Subsequently, the vertical holes are filled with metal (bit lines), and horizontal trenches have alternative stacks of metal layers (word lines) and insulator layers. Domain wall conductive channels can be created and erased between the addressed word and bit lines, as indicated in Figure 5C. In this way, the 3D DWRAM possesses high enough storage capacity to compete with the 3D NAND technology in the future, as shown in Figure 5D.

SUMMARY AND OUTLOOK

Under the electrical stimulation, erasable conductive domain walls appear within an insulating ferroelectric material, promoting the integration of various nano-electronic components, including high-density ferroelectric domain wall memories. This perspective begins with an overview of recent advances in domain and domain wall engineering and then compares the latest architectures and operating principles of emerging domain wall memories. Particular attention is given to large-area LN single-crystal films integrated into silicon wafers that are available in the market now. The persistent internal domains within each LN cell can achieve the memory function, while ultra-thin volatile domains at the interface facilitate a selector in a diode current. The incorporated interface layers can implement logic and selector functions in crossbar memories with excellent reliability, superior to other emerging memories based on polycrystalline thin films. Finally, we briefly discuss three-dimensional stacking of memory cells in the future. For the 3D integration, the main challenge is the fabrication of column arrays within a thick LN single-crystal film with high etching rates, excellent mask selectivity, and near-vertical profiles in high aspect ratios.

Over the past few years, the field of ferroelectric domain walls has grown exponentially, contributing to the rise of domain wall nanoelectronics. Solid-state demonstration devices based on domain wall conductivity show performance that can compete with emerging NVMs on the market, but more maturity is needed to validate the technology from lab to fab. First, considering that commercial SRAM and DRAM operate at > 10^{15} cycles of endurance, sufficiently high endurance cycles must be verified to achieve higher switching cycles at high-speed read and write states. Proven commercial FeRAM can provide up to 10^{14} endurance counts and up to ten years of retention properties over a wide temperature range (-40 to 85 °C), which is also required for domain wall memories. The magnitude of the domain wall current determines the suitability of future domain wall memories for high-speed operation on nanosecond and faster time scales, and strategies include elemental doping control of ion migration (bulk phase *vs.* wall phase control) and reliable generation of CDWs[59]. It should be pointed out here that although CDWs can improve the domain current, their own high depolarization energy is detrimental to the retention performance of the device, so new domain wall engineering strategies are needed to integrate the domain wall current and retention

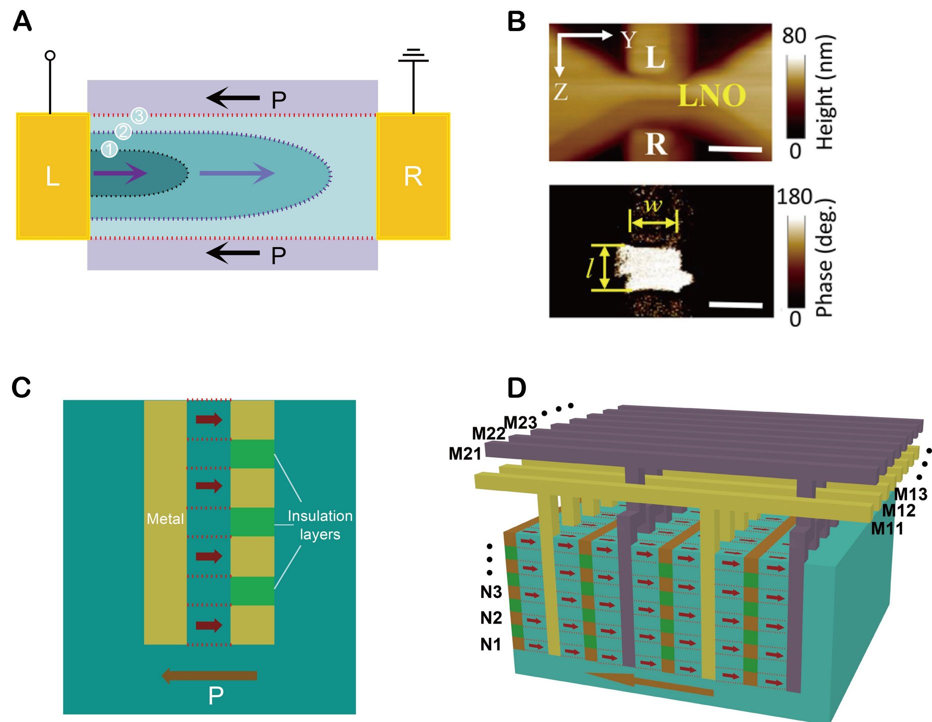

Figure 5. (A) Schematic illustration of the polarization reversal within an LN memory cell. Arrows show domain orientations. (B) AFM topographic mapping of an in-plane LN mesa-like cell in sizes of w × l × h = 200 × 200 × 60 nm^3 (upper panel). The intradomain between L and R can be switched into an opposite direction after the application of a poling voltage of 5 V, as inferred from in-plane PFM phase imaging in the lower panel. Scalar bars, 200 nm. Reprinted with permission[62].Copyright 2022, AIP Publishing. (C) Sectional view of a three-dimensional stack of domain wall memories. (D) Bird's-eye view of a three-dimensional stack of domain wall memories.

performance. Second, the ferroelectric domain walls are only about 1 nm thick, but the cost of erasing and writing the domain walls stems from the magnitude and duration of the applied voltage. In order to accommodate the operating voltages in standard CMOS processes, domain wall memories require further validation of lower operating voltages, with strategies that include validation of more advanced technology nodes and methods to reduce the coercive field of the ferroelectric material itself. Third, the microstructures of the domain walls and domain wall memory cells are very important, including the frameworks, interfaces, and atomic-scale structures. These elements play a crucial role in determining the performance of domain wall memory devices.

In addition, it is also important for different material systems to address the challenges of synthesis and integration. Typical prototype demonstrations of domain wall memories are presented on pulse-deposited BFO films and commercially available LN single-crystal and single-crystal films. The use of self-assembled ferroelectric nano-islands displaying quadrants and/or centrally convergent and divergent domain walls in the BFO thin film material system to achieve vertical-type capacitor geometries is advantageous for the CMOS integration process. However, the problems are the high temperature of film deposition, too small readout domain wall currents, and the fact that competitive endurance and retention properties have not yet been shown. With the maturity of LNOI technology and its application in photonics, the prospect of commercializable domain wall memories in LN systems has increased. Interfacial dead layers act as selective tubes, allowing for low-cost, high-density integration while exhibiting excellent storage performance. However, in terms of the preparation cost of LNOI materials, they are still far from being viable for industrialization unless they are verified to have a significant advantage in terms of storage capacity in

monolayer or multilayer structures. Recently, high-quality self-supported chalcogenide oxide $BaTiO_3$ ferroelectric thin films were prepared on silicon substrates by a growth-transfer method, and erasure and readout of the domain walls were realized by using the head-to-head type CDWs formed in the $BaTiO_3$/Si heterojunction[63]. This integrated scheme is instructive for the development of CMOS process-compatible domain wall memories. However, even though the authors obtained CDWs, the readout current was only on the order of pA[63]. In addition, van der Waals ferroelectric materials[64] with high polarization leading to high charge density at the walls provide additional material options for domain wall-based electronic devices.

DECLARATIONS

Authors' contributions

Organized the literature review and drafted the original version: Sun J
Review and supervision: Li Y, Hu D, Shen B, Zhang B, Wang Z, Tang H
Conceived and supervised the project: Jiang A

Availability of data and materials

Not applicable.

Financial support and sponsorship

This work was supported by the National Key Basic Research Program of China (Grant numbers 2022YFA1402900 and 2019YFA0308500), the National Natural Science Foundation of China (grant number 61904034), and the Ministry of Science and Technology of China (grant number 2022YFA1402904).

Conflicts of interest

All authors declared that there are no conflicts of interest.

Ethical approval and consent to participate

Not applicable.

Consent for publication

Not applicable.

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